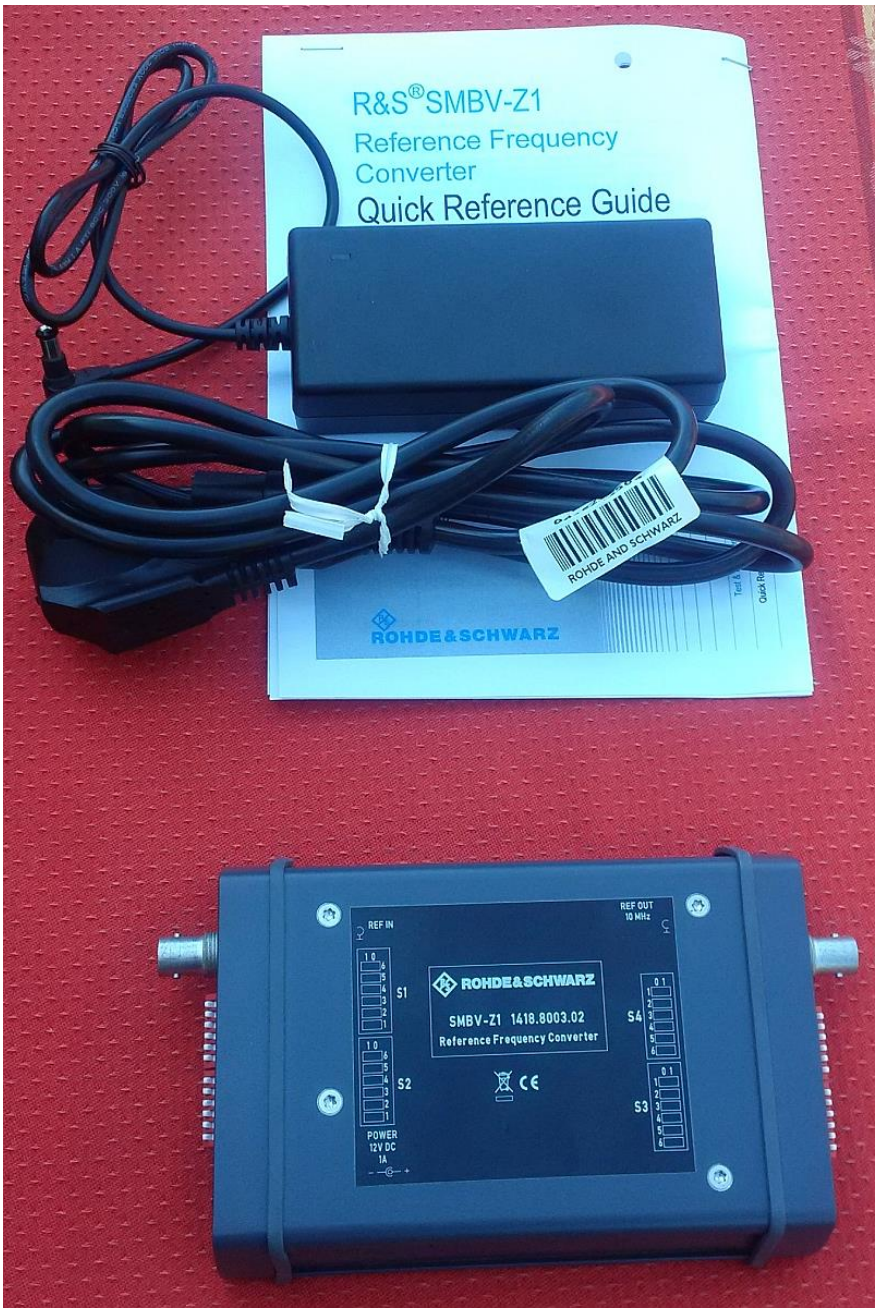
Reference Frequency Converter R&S® SMBV-Z1

Matthias, DD1US, January 22nd 2019, Rev 1.1

Hello,

some time ago I acquired a nice device from Rohde & Schwarz. It is a reference frequency converter which allows to generate a highly precise and low noise 10 MHz reference frequency from a corresponding input signal in a wide frequency range. The SMBV-Z1 translates the input reference signal to the output signal by a phase locked loop (PLL).

Here are some pictures of the device and the supplied 12V power supply:



Input and output connectors are BNC type, on the left is the REF IN port, on the right is the 10 MHz REF OUT port

The encasing is a very rubust aluminium case, typical R&S® quality

The divider ration of the integrated PLL can be defined by the 4x 6-pin-DIP-switches, please find the description how to set them later in this article

The DIP switches are numbered S1 to S4

Below please find a description derived from information of R&S® (from the data sheet and the quick setup guide).

The R&S®SMBV-Z1 reference frequency converter allows a wide range of Rohde & Schwarz signal generators to be synchronized to reference signals of various frequencies. When equipped with this converter, a Rohde & Schwarz signal generator can be referenced to a system's reference signal, even if it is not directly supported by the signal generator's reference input.

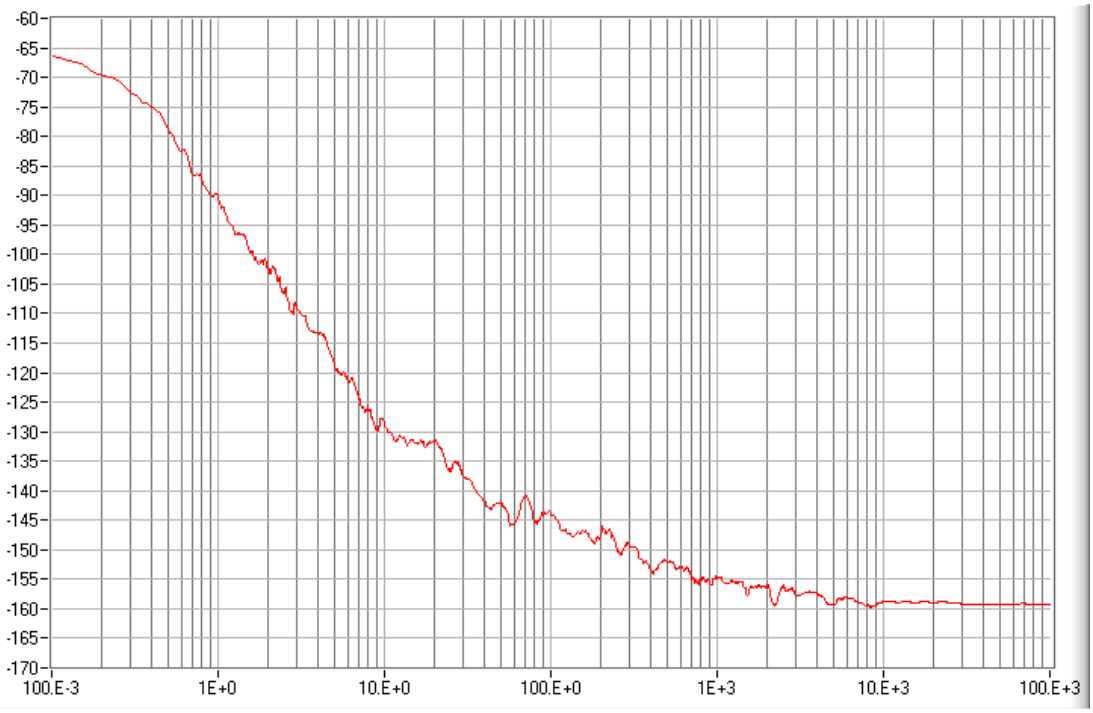
The R&S®SMBV-Z1 reference frequency converter outputs a 10 MHz signal that is phase-locked to the converter's input signal. A narrow phase-lock bandwidth ensures that excessive noise has minimum influence on the input signal so that the signal generator's phase noise performance is maintained. The output of the R&S®SMBV-Z1 should be connected directly to the reference input of the signal generator.

The device is powered by 12V DC and the maximum current consumption is 600 mA. After Warm-up the typical current consumption is 180mA.

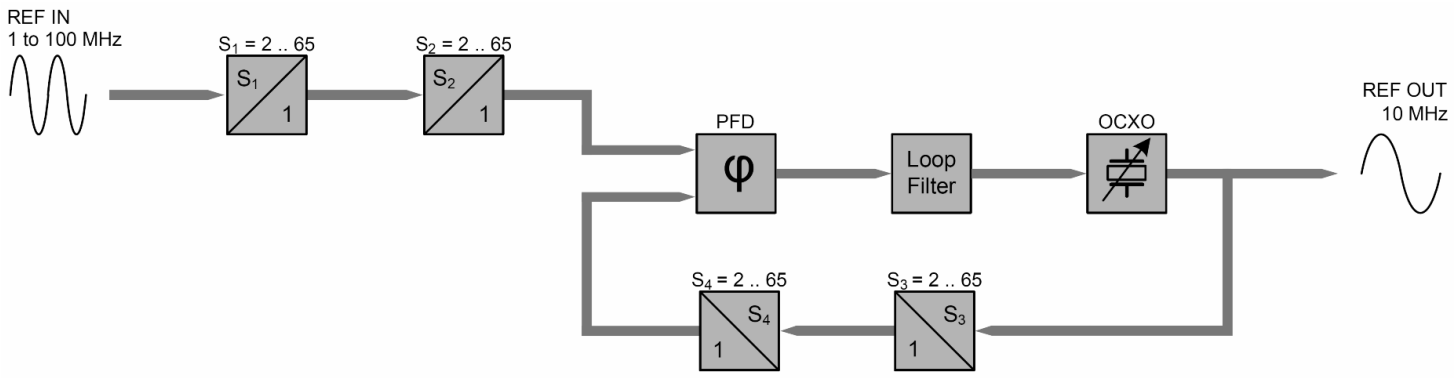
Here are the specifications:

Input frequency range	1 MHz to 100 MHz
Permissible input frequencies	M = 2 to 65, N = 2 to 65, M/N · 10 MHz
Input frequency accuracy	< ±7 × 10–7
Input level	10 dBm to 16 dBm
Input impedance (nom.)	50 Ω
Output frequency	10 MHz (referenced to input signal)
Output level (nom.)	13 dBm
Internal PLL bandwidth (nom.)	0.5 Hz (for 10 MHz/N = 20 kHz)
Setting time (nom.)	< 60 sec (for 10 MHz/N = 20 kHz)

R&S® was kind enough to also provide the measure phase noise of the 10 MHz output signal:



Next you can find the block diagram of the SMBV-Z1 and a short description of its function:



The input signal is scaled in frequency via two serial frequency dividers S1 and S2 and then used as a reference signal for the PLL. The controlled oscillator of this PLL is a low noise OCXO (oven controlled crystal oscillator). Its output signal is split into two paths. One is available at the REF OUT output of the R&S®SMBV-Z1, the other is scaled to the same frequency as the input signal – again using two serial frequency dividers S3 and S4. The scaled down signals are compared at a digital phase detector (PFD).
The Loop bandwidth is in the range of a few Hz, depending on the comparison frequency at the PFD.

So, how to calculate the divider factors and the corresponding settings of the DIP-switches S1 to S4 ?

The R&S®SMBV-Z1 can be set to translate input frequencies to 10 MHz that fulfill the following relation:

$$F_{IN} = \frac{S_1 \cdot S_2}{S_3 \cdot S_4} \cdot 10\,\text{MHz}$$

The division factors S1, S2, S3 and S4 can be set to integer values between 2 and 65.
The divided signal at the phase detector (PFD in the block diagram) should have a frequency FPD in the range of 5 kHz to 100 kHz. The division factors S1 to S4 have to be chosen accordingly.

$$F_{PD} = \frac{F_{IN}}{S_1 \cdot S_2} = \frac{10\,\text{MHz}}{S_3 \cdot S_4} = 5\,kHz \ldots 100\,kHz$$

It is recommended to set S1 to S4 so that FPD is close to 20 kHz. The R&S®SMBV-Z1 Configuration Software can be used to determine suitable values for the division factors S1 to S4.

Finally, here are some examples how to set the divider factors and the corresponding DIP-switches depending on the input frequencies:

Configuration examples				
fin (MHz)	S1	S2	S3	S4
12.288	16_d 010000_b	48_d 110000_b	25_d 011001_b	25_d 011001_b
13.000	13_d 001101_b	50_d 110010_b	50_d 110010_b	10_d 001010_b
15.000	15_d 001111_b	50_d 110010_b	50_d 110010_b	10_d 001010_b
19.200	20_d 010100_b	48_d 110000_b	50_d 110010_b	10_d 001010_b
26.000	26_d 011010_b	50_d 110010_b	50_d 110010_b	10_d 001010_b

Recently I bought a rubidium frequency standard with an output frequency of 8.192 MHz. Using the SMBV-Z1 I am converting this to 10 MHz and feed it to my test equipment. The settings are:
S1=32=100000,
S2=16, 010000,
S3=25=011011,
S4=25=011011

Please note that at the DIP-switches the binary numbers have to be inserted as such:

Bit	DIP-Switch-Position
1	6
2	5
3	4
4	3
5	2
6	1

For instance, for 32=100000 the DIP- switch position 6 has to be set to 1, all others to 0.

If you have any comments or further information then please send them to the Email address given below. Many thanks in advance for your feedback.

Best regards

Matthias Bopp

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